REMARKS

Reconsideration of the application is requested.

Claims 1-3 and 5-23 are now in the application. Claims 1-3 and 5-23 are subject to examination.

Under the heading "Claim Rejections – 35 USC § 103" on page 2 of the above-identified Office Action, claims 1-3, 5, 6, 11-15, 18, and 20-23 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess in view of U.S. Patent No. 5,150,471 to Tipon et al. under 35 U.S.C. § 103. Applicant respectfully traverses.

Claim 1 includes a step of providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule.

Claim 11 includes a hardware address computation circuit for, taking the base address as a starting point, applying an arithmetic computation rule to produce a plurality of addresses used by the digital processor to consecutively access said table memory; said arithmetic computation rule being an incrementation rule or a decrementation rule.

The Examiner has alleged that the ALU would provide a computation rule in order to compute addresses. Column 5, lines 63 to 66 of Hess teach, "The

data to be processed, which has been stored in the main memory AKU, is transferred to the arithmetic logic unit ALU via the 4 bit data bus and is processed in accordance with the operation command". From Fig. 1 and its description it becomes apparent that there is a data exchange between the AKU and the ALU. Hess, however does not teach that the ALU uses any type of arithmetic computation rule to compute addresses. Applicant points out that the ALU in Hess simply processes data that is received from the main memory AKU. The ALU taught by Hess does not even compute addresses.

Additionally, claims 1 and 11 specify that the arithmetic computation rule is provided as an incrementation rule or a decrementation rule. In the response to arguments section on pages 9 and 10 of the Office Action, the Examiner has stated, "... it is well known to one of ordinary skill in the art that the Arithmetic Logic Unit must provide the arithmetic computation basic rules such as incrementation or decrementation rule in order to compute data, address, etc." In response to this statement, applicant wants to emphasize that even if the ALU is capable of applying an incrementation or decrementation rule, this does not necessarily mean that the ALU actually does apply such a computation rule. Hess does not disclose providing an arithmetic computation rule as an incrementation rule or a decrementation rule. Additionally, as already pointed out, the ALU does not compute addresses.

Tipon et al. do not disclose the above-cited features either. Fig. 1 of Tipon et. al. shows an ALU that provides physical addresses by combining base

addresses and offset addresses. This technique does not correspond to the required feature of providing an arithmetic computation rule as an incrementation rule or a decrementation rule.

None of the cited references provide any teaching or suggestion to employ an incrementation rule or a decrementation rule for computing addresses. As matter of fact, the ALU of Hess does not even compute addresses at all. Therefore, even if one of ordinary skill in the art would have combined the teachings of Hess and Tipon et al., all of the features in claims 1 and 11 would not have been taught or suggested.

Let us now consider claims 3 and 13. Claim 3 defines a step of prescribing the plurality of base addresses unalterably in hardware, wherein the plurality of base addresses cannot be processed by the digital processor. Claim 13 specifies that said base address memory device is a read only memory and the plurality of base addresses cannot be processed by the digital processor.

The Examiner has alleged that Tipon et al. teach the copied features of claims 3 and 13 and has referred to column 4, lines 5 to 15, which teach a hard-wired base register 18. In this regard, applicant points out that the mere fact that the base register 18 is "hardwired" does not mean that the base addresses are "unalterably prescribed in hardware".

Column 3, lines 22 to 26 of Tipon et al. teach, "The base address register 18 is loaded by the processor 12 with a preselected, 32 bit base address ... under the control of the processor". If the addresses of the base address register 18 were unalterable in hardware, it would simply not be possible to load the base register 18 with an address. Tipon et al. therefore cannot teach the above cited feature defined in claim 3. A similar argument holds true for claim 13.

Let us now consider claims 21 and 23. Claim 21 defines a hardware counter implementing said arithmetic computation rule as an incrementation rule or a decrementation rule. Claim 23 defines performing the step of providing the arithmetic computation rule by providing a hardware counter that implements the incrementation rule or the decrementation rule.

Applicant has already pointed out that the prior art does not disclose applying an incrementation rule or a decrementation rule in the discussion provided with regard to claim 1. With regard to claims 21 and 23 applicant also points out that the prior art does not teach a hardware counter to implement such a computation rule.

Under the heading "Claim Rejections – 35 USC § 103" on page 6 of the above-identified Office Action, claim 7 has been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess in view of U.S. Patent No. 5,150,471 to Tipon et al. and further in view of U.S. Patent No. 3,833,888 to Stafford et al. under 35 U.S.C. § 103.

Even if Stafford et al. does teach the subject matter that the Examiner has alleged and even if it would have been obvious to combine the teachings of the references, the invention as defined by claim 7 would not have been obtained for the reasons specified above with regard to claim 1 and the deficiencies in the teachings of Hess and Tipon et al.

Under the heading "Claim Rejections – 35 USC § 103" on page 8 of the above-identified Office Action, claims 8 and 19 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess in view of U.S. Patent No. 5,150,471 to Tipon et al. and further in view of U.S. Patent No. 5,311,523 to Serizawa et al. under 35 U.S.C. § 103.

Even if Serizawa et al. does teach the subject matter that the Examiner has alleged and even if it would have been obvious to combine the teachings of the references, the invention as defined by claims 8 and 19 would not have been obtained for the reasons specified above with regard to claims 1 and 11 and the deficiencies in the teachings of Hess and Tipon et al.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 11. Claims 1 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 11.

Finally, applicant appreciatively acknowledges the Examiner's statement that claims 9, 10, 16, and 17 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above discussion, however, applicants respectfully believe that rewriting of claims 9, 10, 16, and 17 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-3 and 5-23 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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